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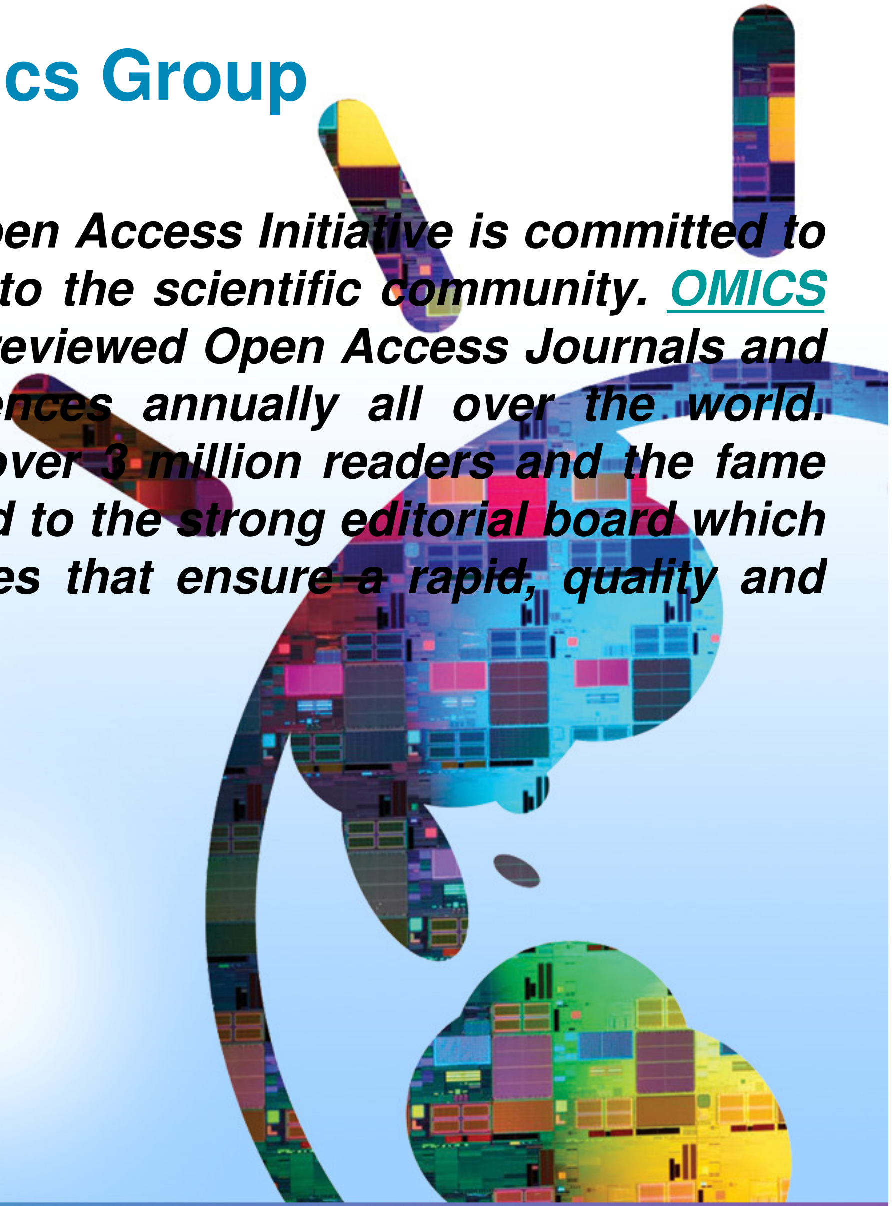

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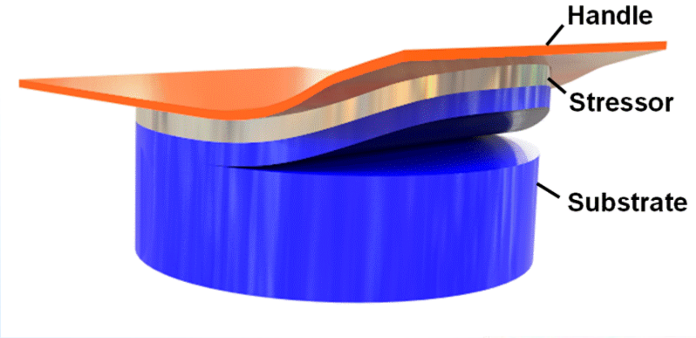
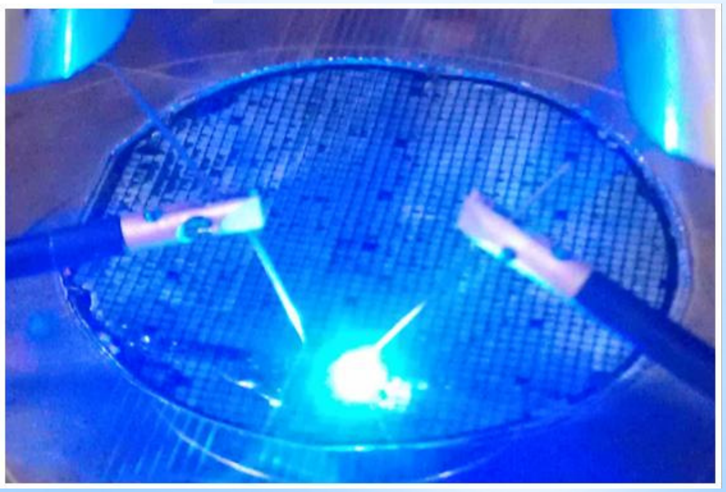
New Approach to Low-Cost Solid State Lighting Using Controlled Spalling

Stephen W. Bedell
IBM T. J. Watson Research Center





S. W. Bedell, K. Fogel, P. Lauro, C. Bayram, D. Shahrjerdi, J. Kiser, J. Ott, Y. Zhu and D. K. Sadana

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Outline

- Vertical LEDs for high-performance lighting – the need for GaN layer transfer.
- Limitations of present layer transfer methods
- Controlled spalling technology
- Application of Controlled Spalling to GaN
- Other applications of spalling
- Conclusions

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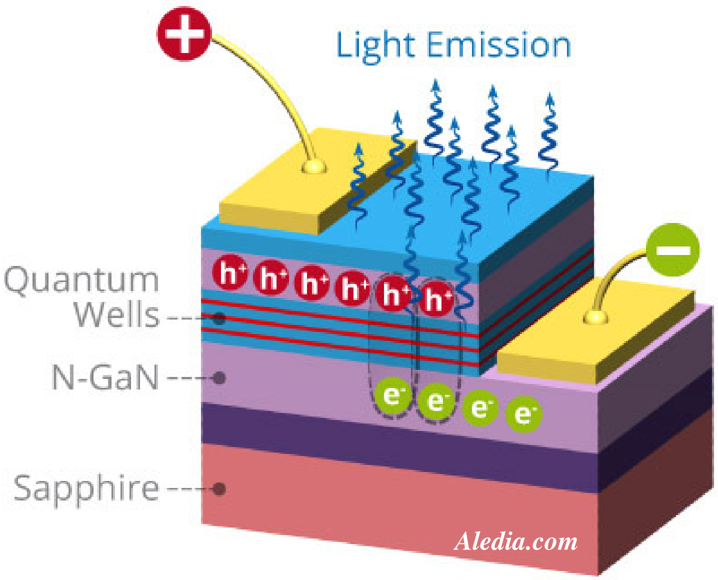
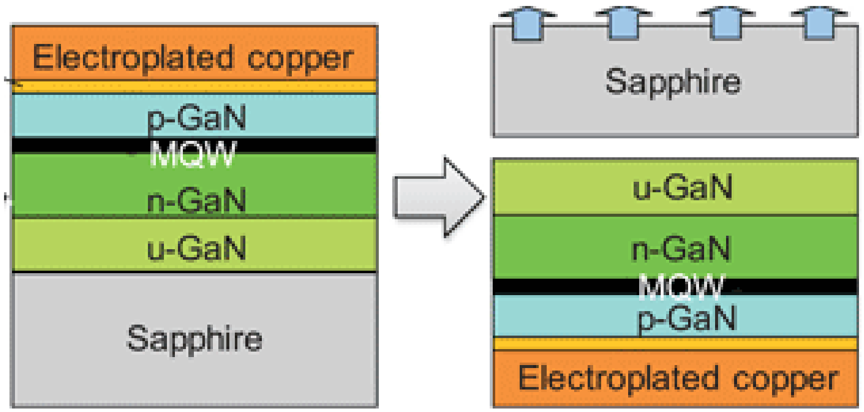
Vertical LEDs for High-Performance Solid-State Lighting





Deposit or bond metallic superstrate

Remove growth substrate

Adapted from Wong *et al.*, *Appl. Phys. Lett.* (2012)

Conventional LED

- Inexpensive
- Relatively easy to fabricate
- Current crowding in n-GaN
- Poor current spreading in p-GaN
- Poor thermal performance (Al_2O_3)
- Limited light extraction

Vertical LED

- Superior contact to p-GaN
- Better current spreading
- Better light extraction (mirror)
- Much better thermal performance
- Need to remove substrate
- Higher cost / lower yield

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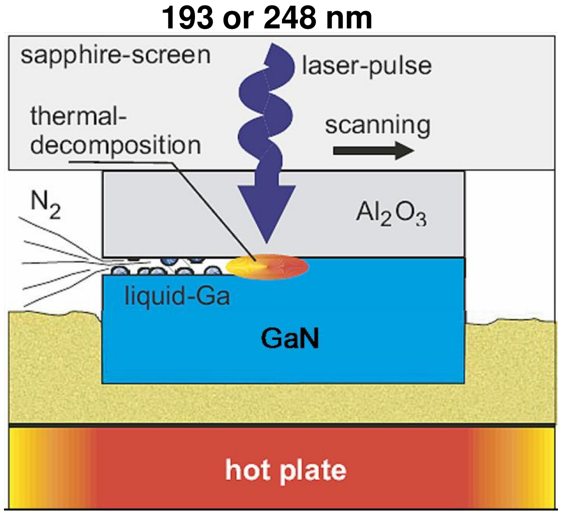
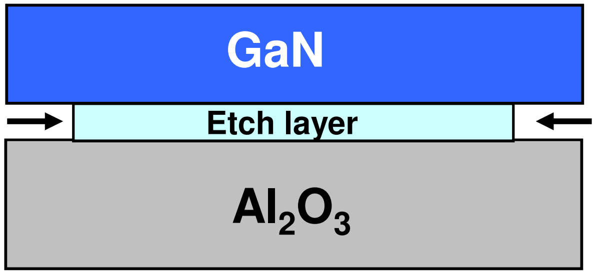
Existing GaN layer transfer methods



phys. stat. sol. (2006)



Laser Lift-Off (LLO)

- Most VLEDs use this method
- Commercial tools / processes available
- Narrow process window
- Only works for GaN on Al_2O_3
- Even GaN on PSS is challenging
- Can only separate at GaN/Al_2O_3 interface

Chemical Lift-Off (CLO)

- Allows control over separation depth
- Batch processing possible
- CrN, GaN:Si, ZnO and Porous GaN have been demonstrated.
- CLO necessarily complicates growth and performance of overgrown devices.
- Large-area CLO difficult in practice
- Etch time diverges for larger wafer diameters.

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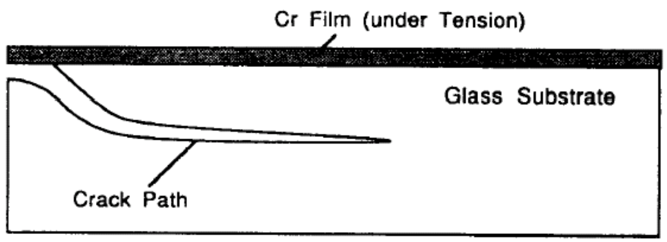
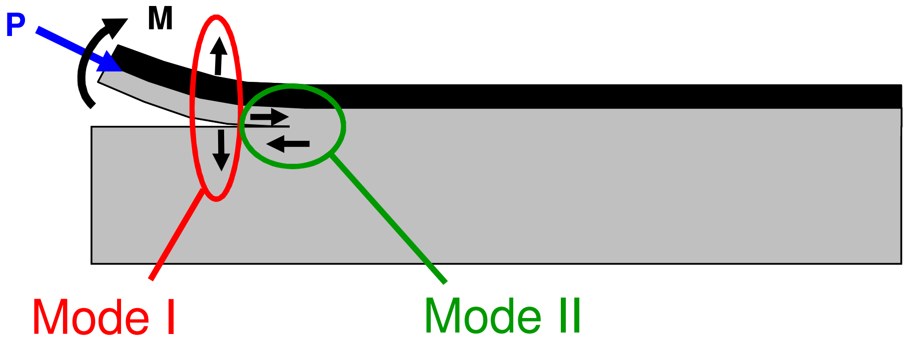
Spalling is a unique mode of brittle fracture whereby a tensile surface layer induces fracture parallel (and below) the film/substrate interface.

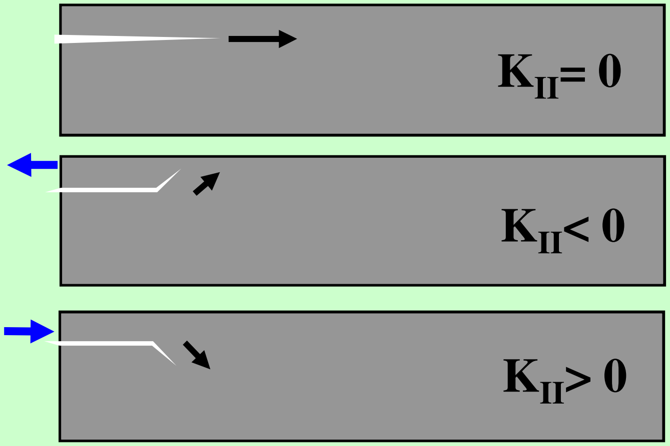
Observed behavior



From Suo and Hutchinson (1989)

The origin of this effect lies in the combination of normal stress (type I) and shear stress (type II).





Adapted from Thouless et al. (1987)

The effect of the shear stress (K_{II}) is to defect the crack in the direction which minimizes shear ($K_{II} = 0$). For a compressive layer, the crack will deflect up and crack the layer. For a tensile layer, the crack will deflect into the substrate to a depth where $K_{II} = 0$. The crack trajectory is stable because K_{II} is *corrective*.

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Challenges with spalling mode fracture as a layer transfer technology

- Generally, spalling is a **spontaneous**, **uncontrolled**, **failure mode** that is accompanied by concurrent fracture modes (film cracking, channel cracking, substrate breakage, etc.)

- Spontaneous (self-initiated) spalling leads to **multiple crack fronts** that lead to fracture instability where they meet.

- **Stress is often related to thermal effects** (CTE differences, etc.) that limit the types of structures that can be spalled. Moreover, dislocations can propagate at even modest temperatures (~400° C in Si).

- **Little ability to engineer or design a process** (layer thickness, residual stresses, etc.).

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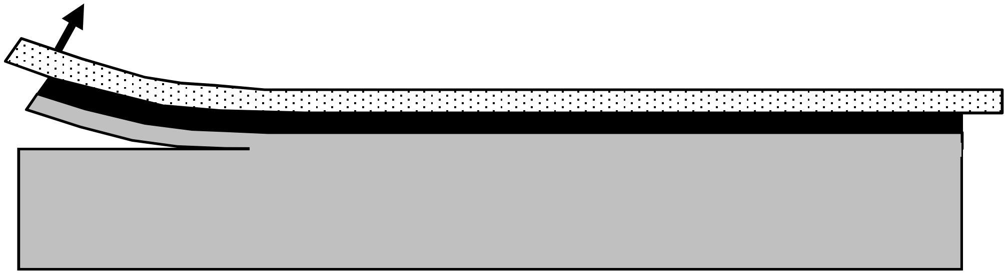
What is controlled spalling?

Intrinsic stress is used to drive fracture, and the crack front is mechanically guided.

Deposit stressed layer onto substrate to a thickness near the critical condition.

Apply a handling layer. Tape works but it must be thin in order not to change the critical conditions too drastically.



Initiate fracture at one edge of the substrate, and propagate fracture front uniformly across surface.

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Controlled spalling dramatically increases the versatility and usefulness of low-cost layer transfer.

- Because the entire process can be performed at ***room temperature***, we can apply this technique to a wide range of materials including finished devices.

- **Depth control:** We can engineer the stress of the layer in order to design the critical thickness which, in turn, establishes the fracture depth.

- A single fracture front drastically improves yield, roughness, and wafer reusability.

- We can *combine controlled spalling* with ***engineered fracture layers***, as well **as *etch stop layers***, for atomic-level control of layer thickness.

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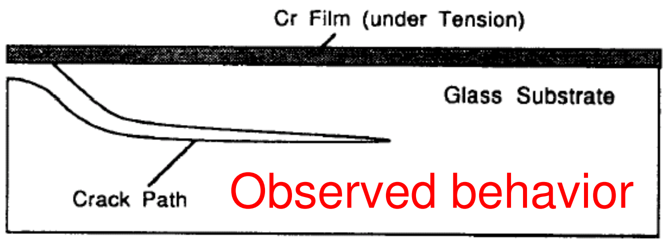
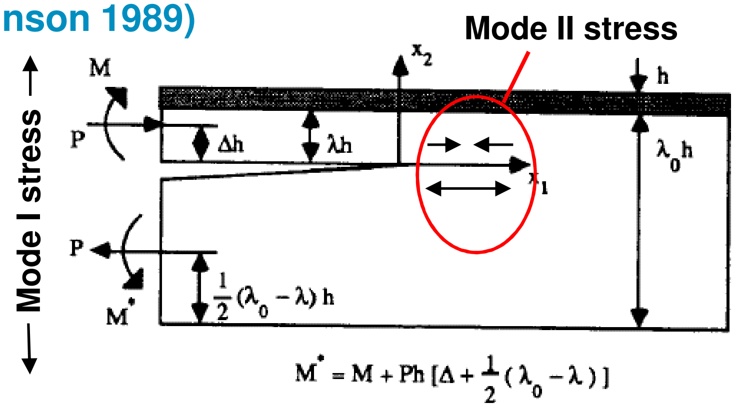
Mixed mode fracture: Spalling

(from Suo and Hutchinson 1989)



Observed behavior



$$M^* = M + Ph\,[\Delta + \frac{1}{2}(\lambda_0 - \lambda)]$$

Mechanical model

$$K_{\mathrm{I}} = \frac{P}{\sqrt{2Uh}}\cos\omega + \frac{M}{\sqrt{2Vh^3}}\sin(\omega+\gamma)$$

$$K_{\mathrm{II}} = \frac{P}{\sqrt{2Uh}}\sin\omega - \frac{M}{\sqrt{2Vh^3}}\cos(\omega+\gamma)$$

Mechanical analysis

$$\Delta = \frac{\lambda^2 + 2\Sigma\lambda + \Sigma}{2(\lambda+\Sigma)}, \quad \Delta_0 = \frac{\lambda_0^2 + 2\Sigma\lambda_0 + \Sigma}{2(\lambda_0+\Sigma)}$$

$$I = \{\Sigma[3(\Delta-\lambda)^2 - 3(\Delta-\lambda) + 1] + 3\Delta\lambda(\Delta-\lambda) + \lambda^3\}/3$$

$$I_0 = \{\Sigma[3(\Delta_0-\lambda_0)^2 - 3(\Delta_0-\lambda_0) + 1] + 3\Delta_0\lambda_0(\Delta_0-\lambda_0) + \lambda_0^3\}/3$$

$$P = P_1 - C_1 P_3 - C_2\frac{M_3}{h}, \quad M = M_1 - C_3 M_3$$

$$C_1 = \frac{A}{A_0}, \quad C_2 = \frac{A}{I_0}[(\lambda_0-\Delta_0)-(\lambda-\Delta)], \quad C_3 = \frac{I}{I_0}$$

$$A = \lambda + \Sigma, \quad A_0 = \lambda_0 + \Sigma$$

Fracture trajectory occurs where K_{II} = 0

minimize K_{II} w.r.t. crack depth (λh)

Use result to solve K_I and compare to fracture toughness to see if spalling is spontaneous.

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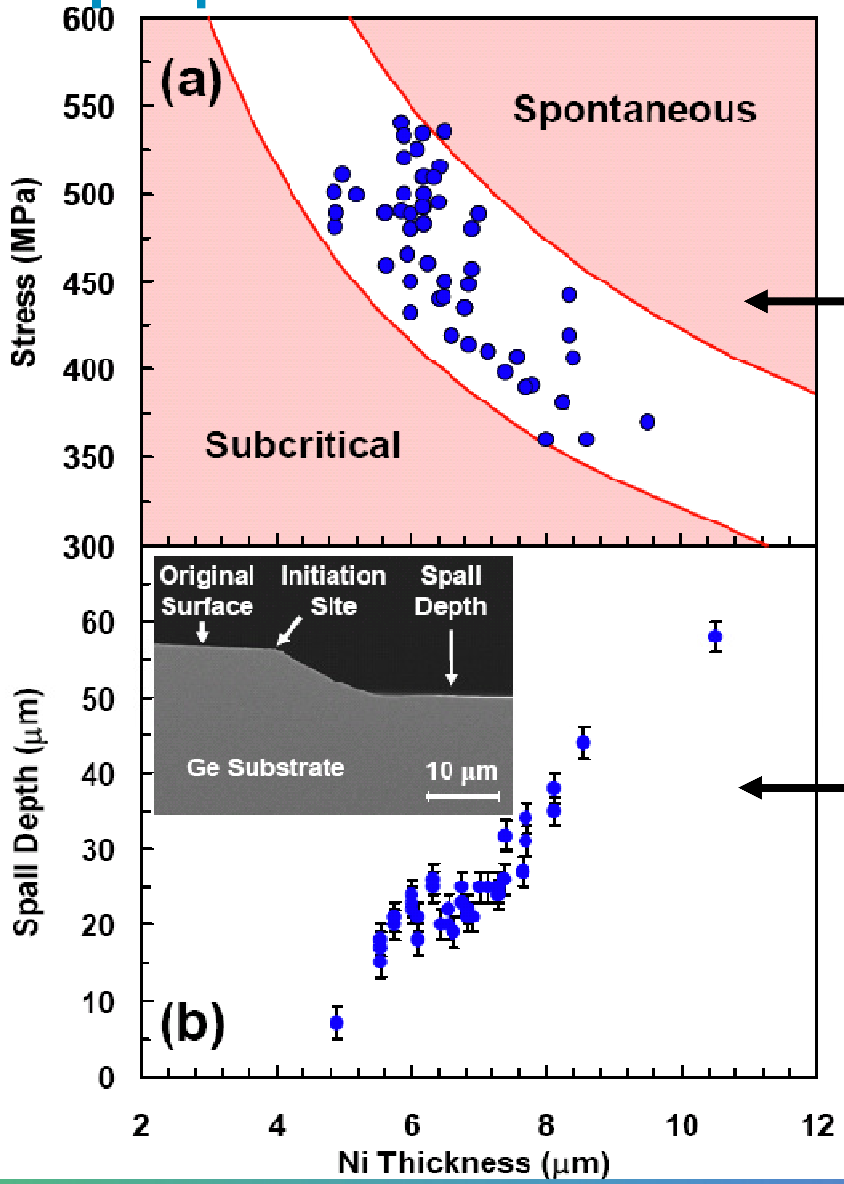
Example process window for Ge<001> substrates

Bedell *et al.*, *J. Phys. D: Appl. Phys.* **46** (2013) 152002



Stress is controlled to ensure metastability of fracture.

Desired spall depth dictates a given Ni thickness

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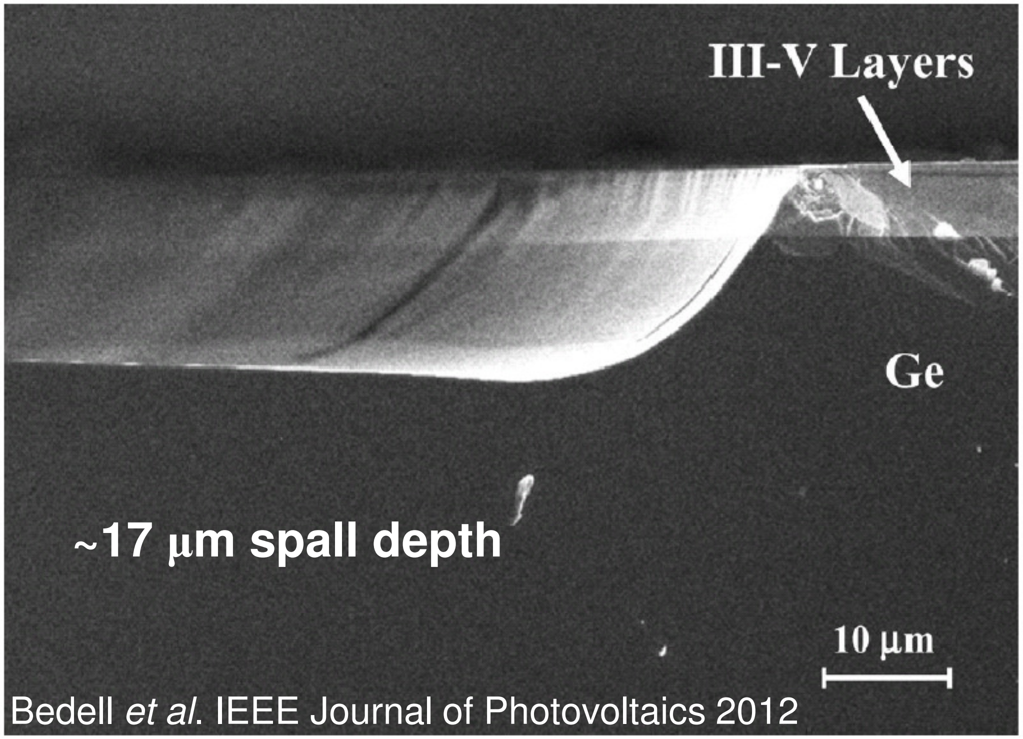
Getting the crack started



Bedell *et al*. IEEE Journal of Photovoltaics 2012

In Controlled Spalling, there is no spontaneous fracture, therefore a crack must be introduced at the edge of the wafer.

The simplest way to achieve this is to create an abrupt stress discontinuity in the stressor layer. By applying the handle layer and exerting a small force, a crack is formed in the substrate.

- Create an abrupt stress discontinuity in the Stressor (Ni) near wafer edge.
- Apply handle layer (e.g., tape)
- Lift tape causing a crack to form in the substrate at the Ni edge.

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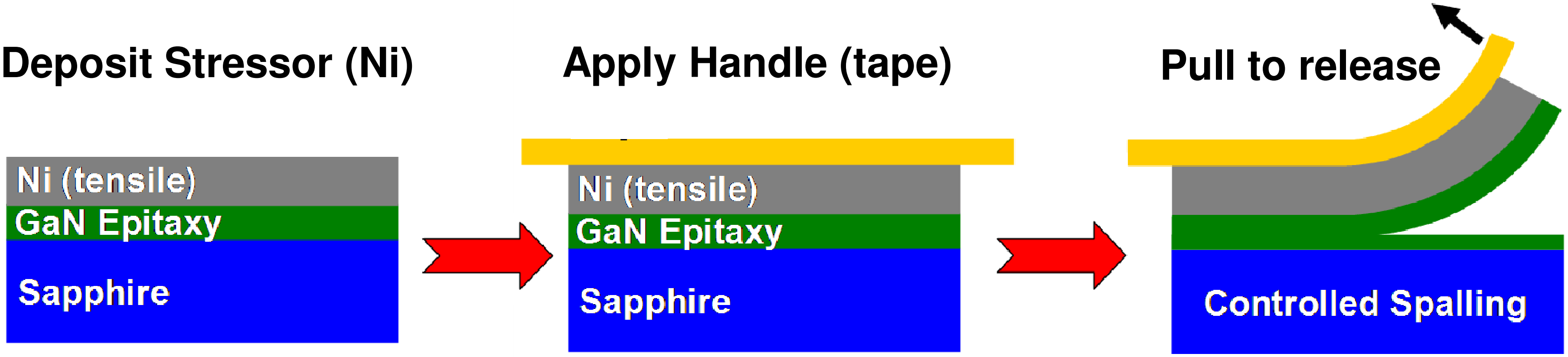
Process for Controlled Spalling of GaN on planar Al_2O_3

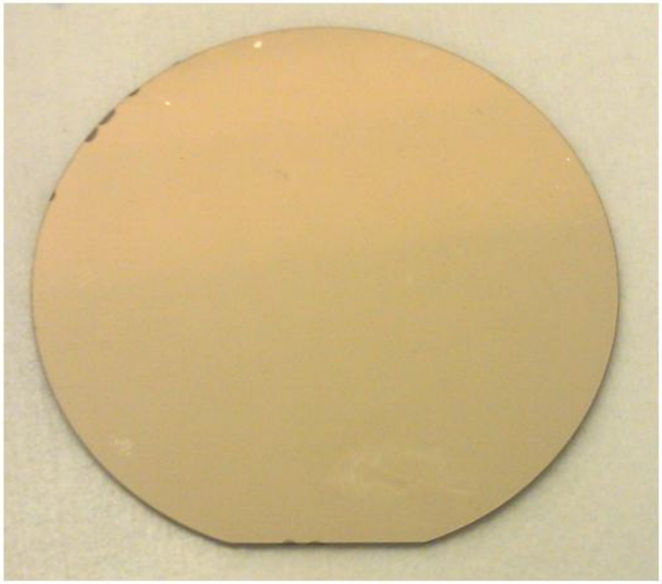


Deposit Stressor (Ni)

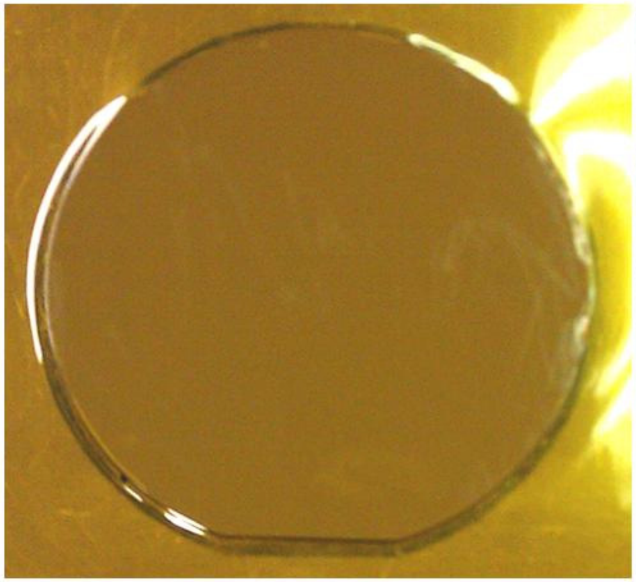
Apply Handle (tape)

Pull to release

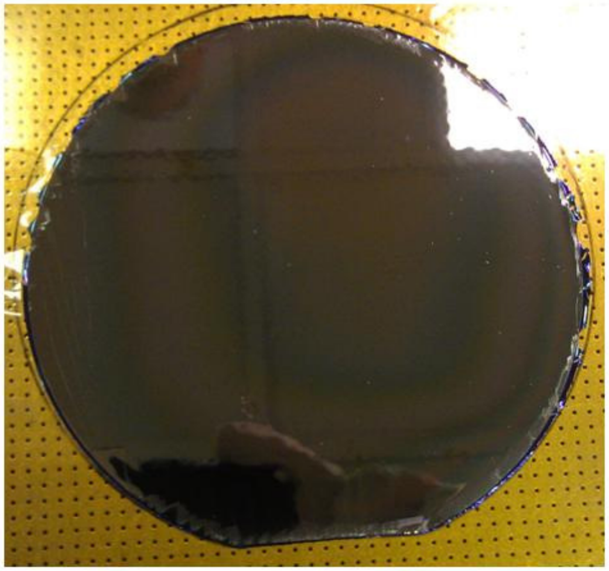
Electroplated Ni on GaN/Al_2O_3



Roll-applied Kapton tape



LED/GaN epitaxy removed



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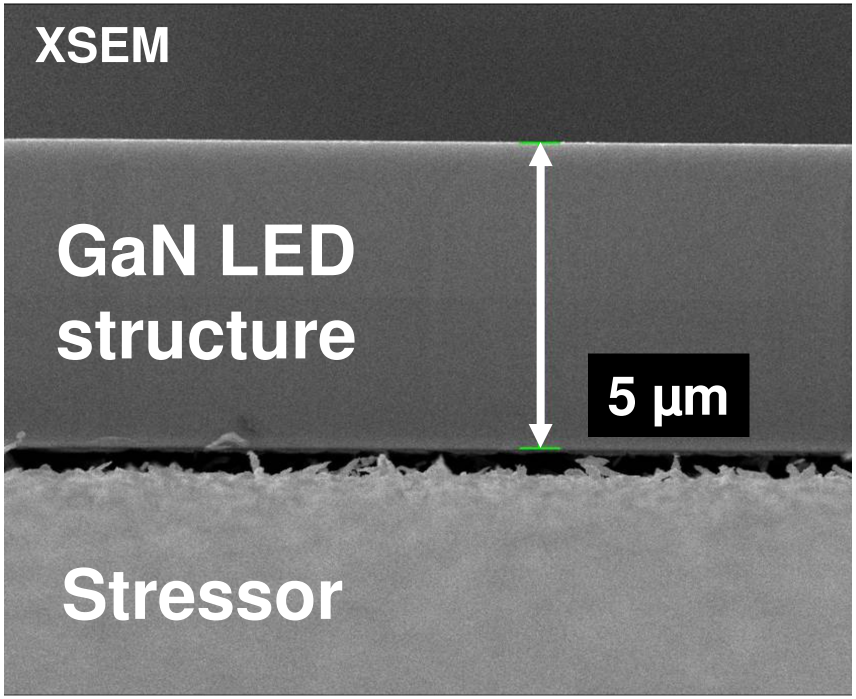
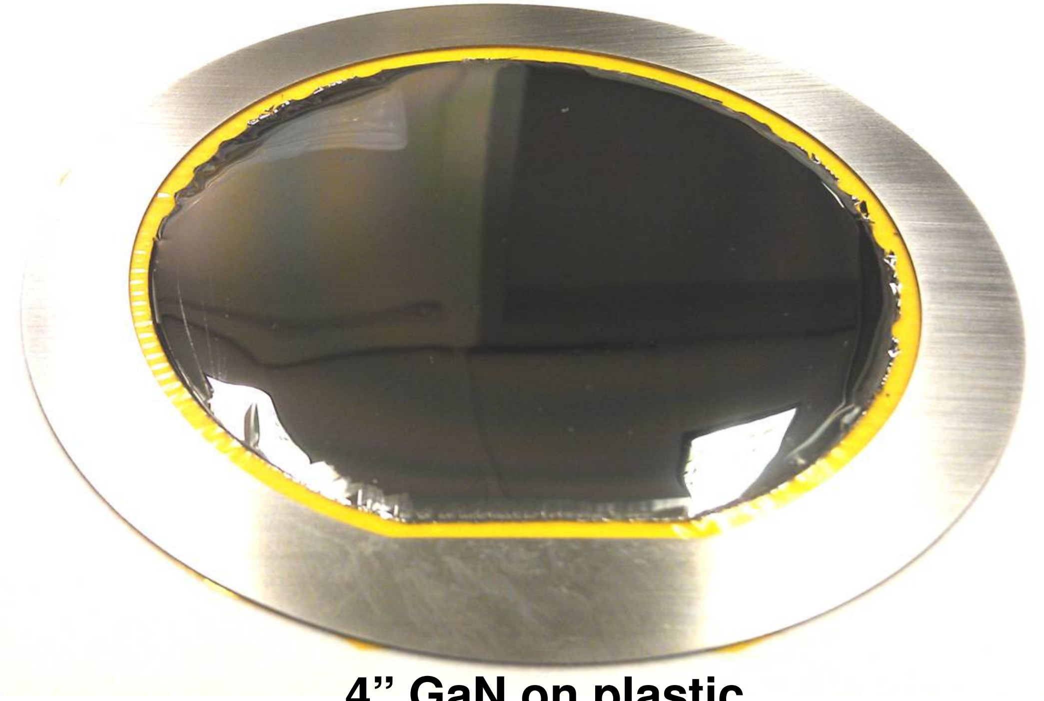
Wafer scale transfer of GaN





4” GaN on plastic

- CST has been used for wafer-scale transfer of GaN grown on Al_2O_3, PSS, Si and bulk GaN.

- It is even possible to perform CST with contact metallization in place.

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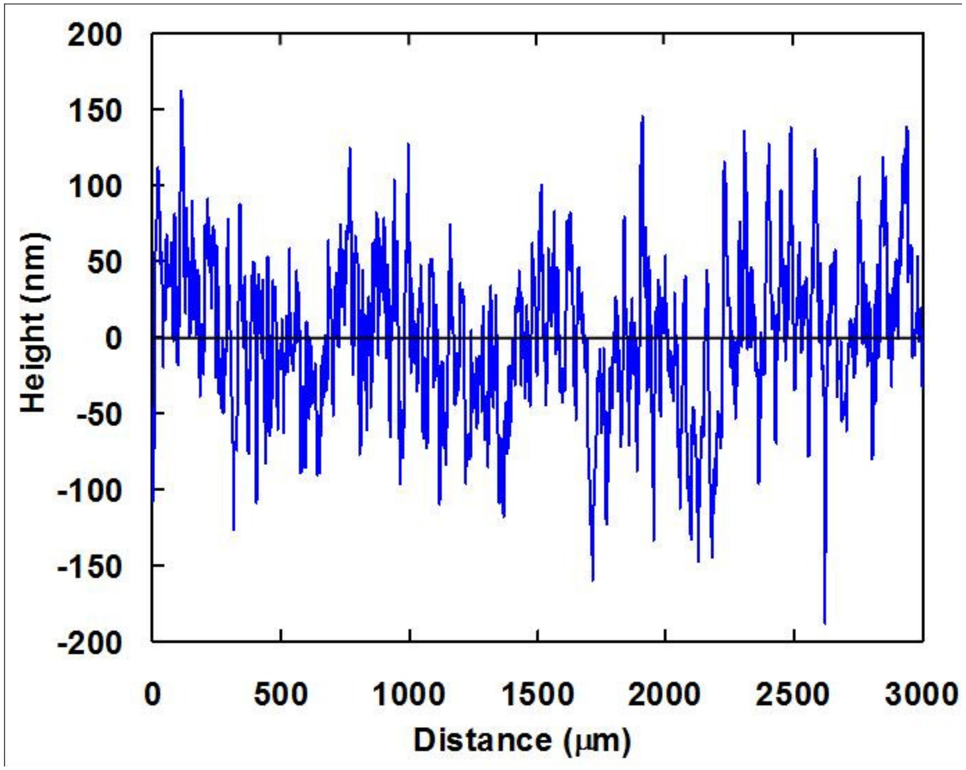
Demonstration of spalled, flexible, green LEDs

- Green InGaN/GaN MQW structures grown on 2” PSS sapphire wafers
- 25 µm, 400 MPa Ni was electrodeposited onto structure
- Kapton tape was applied and used to guide fracture

2” spalled InGaN/GaN layers

Profilometry of spalled surface



S.W. Bedell, *et. al.* Appl. Phys. Express (2013)

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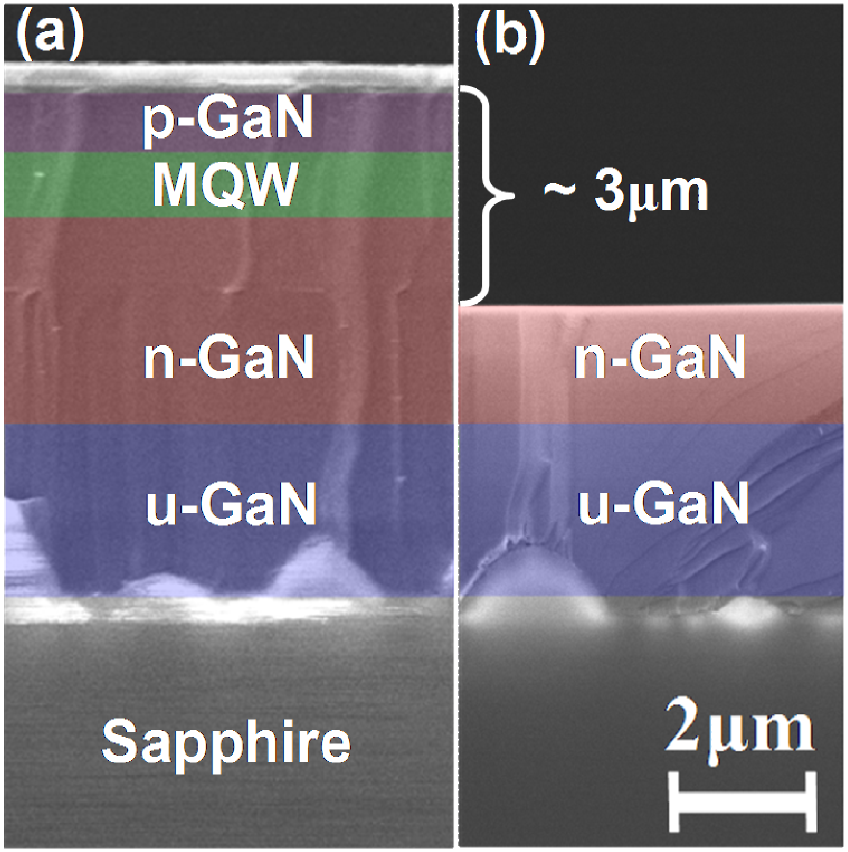
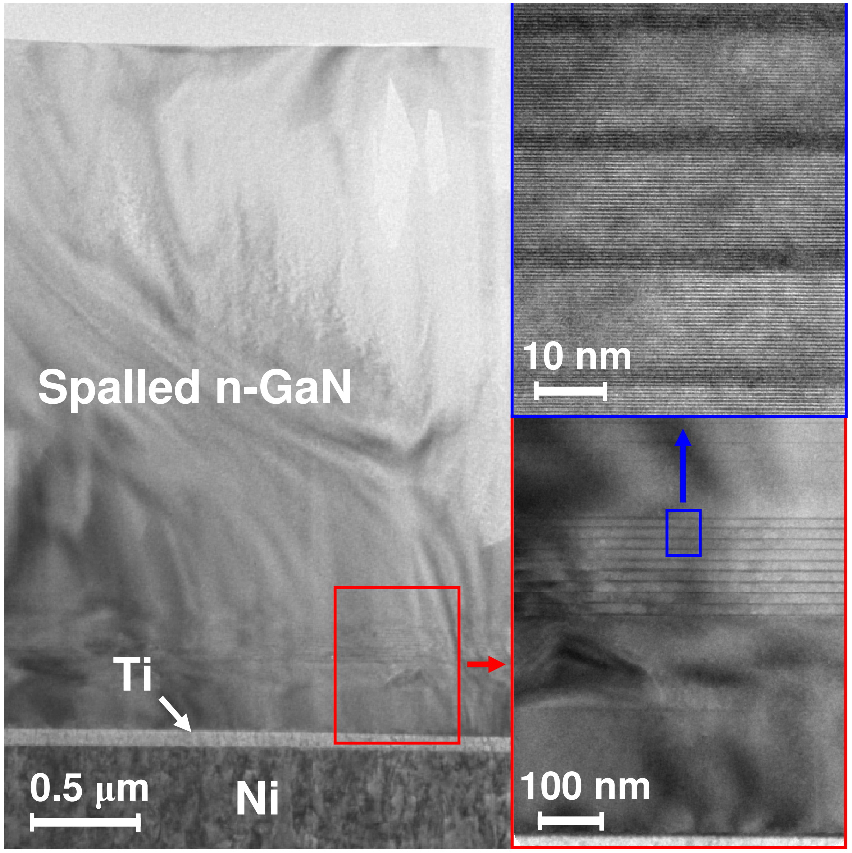
Structural characterization of spalled LEDs (SLEDs)

XSEM image showing ~ 3µm spall depth



XTEM image showing no spalling-related lattice damage



S.W. Bedell, *et. al*. Appl. Phys. Express (2013)

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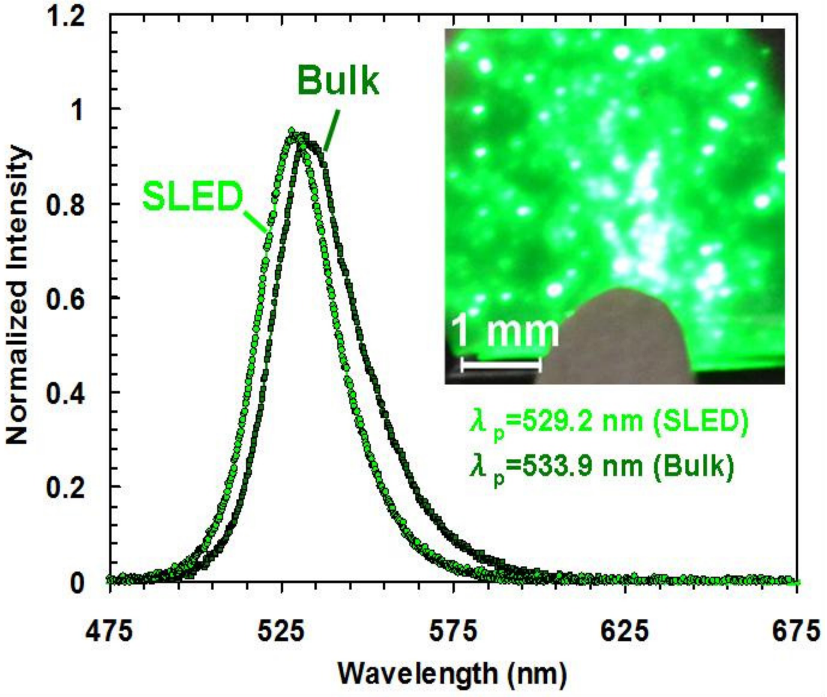
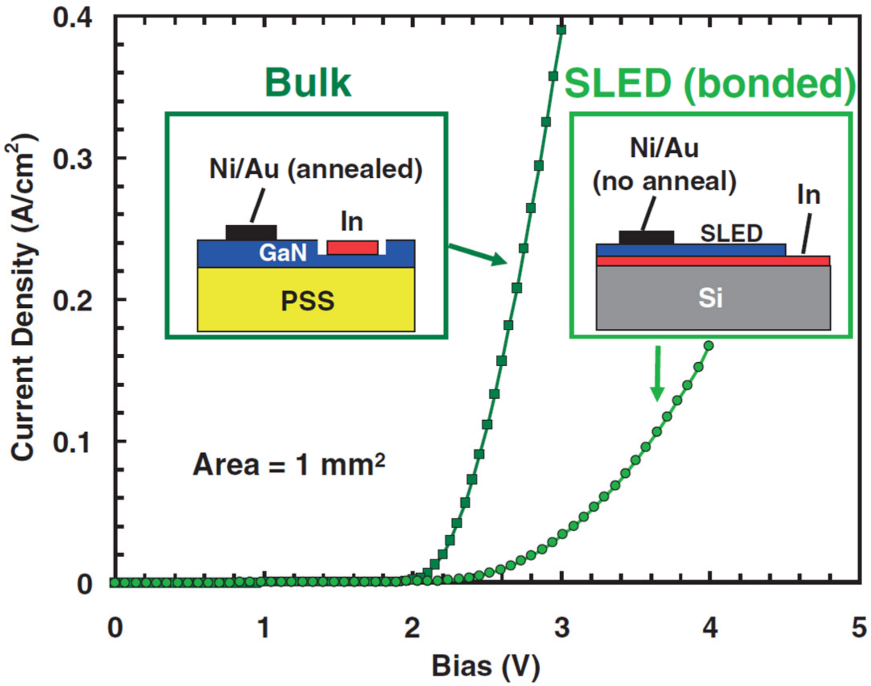
Electrical characteristics of SLEDs

Due to exposed n-GaN, the as-spalled layers could be probed directly.

EL data from as-spalled layers:



In order to measure the J-V characteristics of the SLED devices, the layers were bonded to Si and the Ni layer was removed.



Similar V_F, but higher series resistance due to non-annealed contacts.

S.W. Bedell, *et. al*. Appl. Phys. Express (2013)

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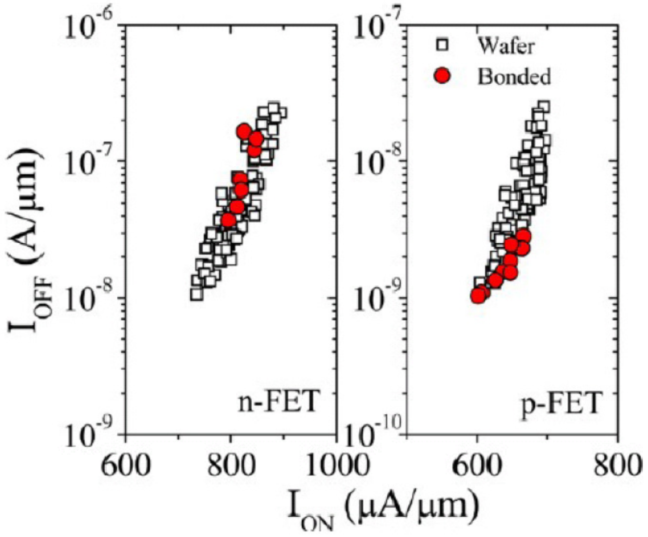
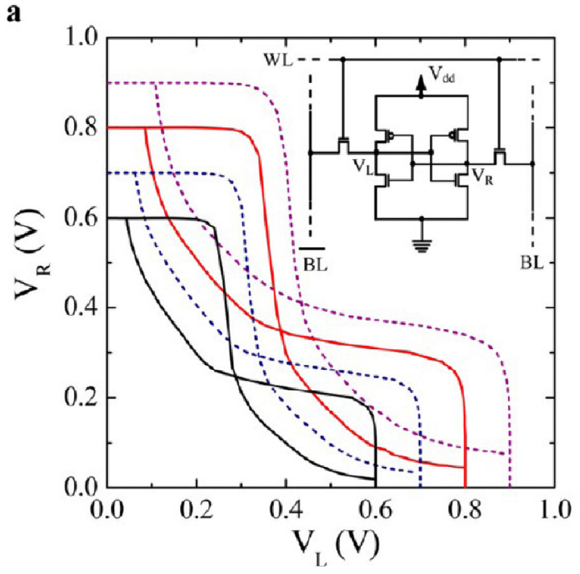
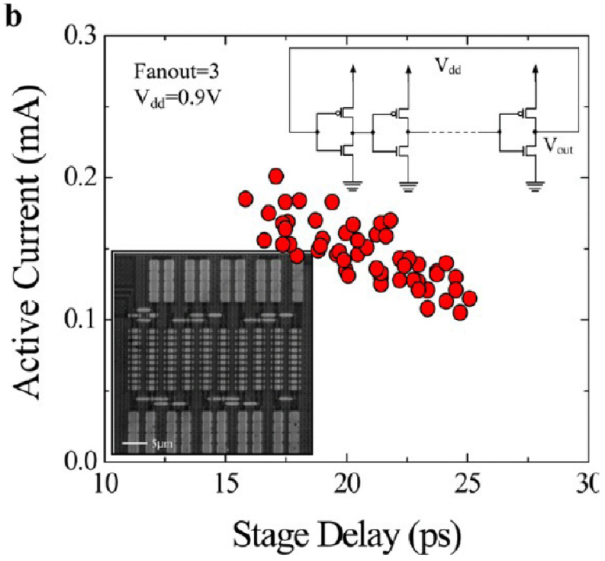
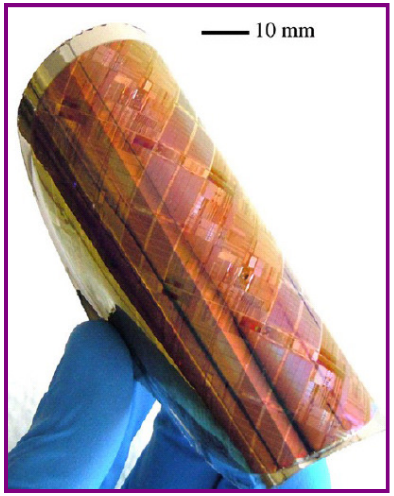
Electrical characteristics of spalled circuits

Shahrjerdi & Bedell *NanoLett*. **13** (2013) 315









- Devices functional and equivalent after spalling
- 6T SRAM functional down to 0.6 V.
- 100 stage RO with stage delay of ~16ps
- Other opportunities (backside SIMS / TEM prep.)

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Flexible Photovoltaics

- In many applications, what matters most for a photovoltaic system is power under weight or area constraint.

- Examples of these applications are aerospace, military and consumer portable products.

- By spalling III-V based multijunction solar cells we can create lightweight and flexible devices with high conversion efficiency.

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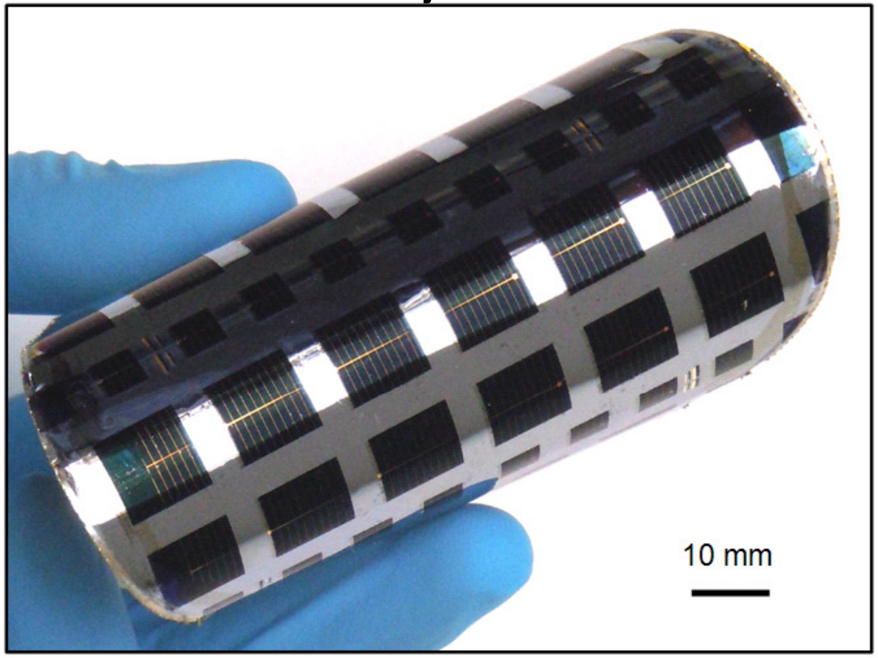
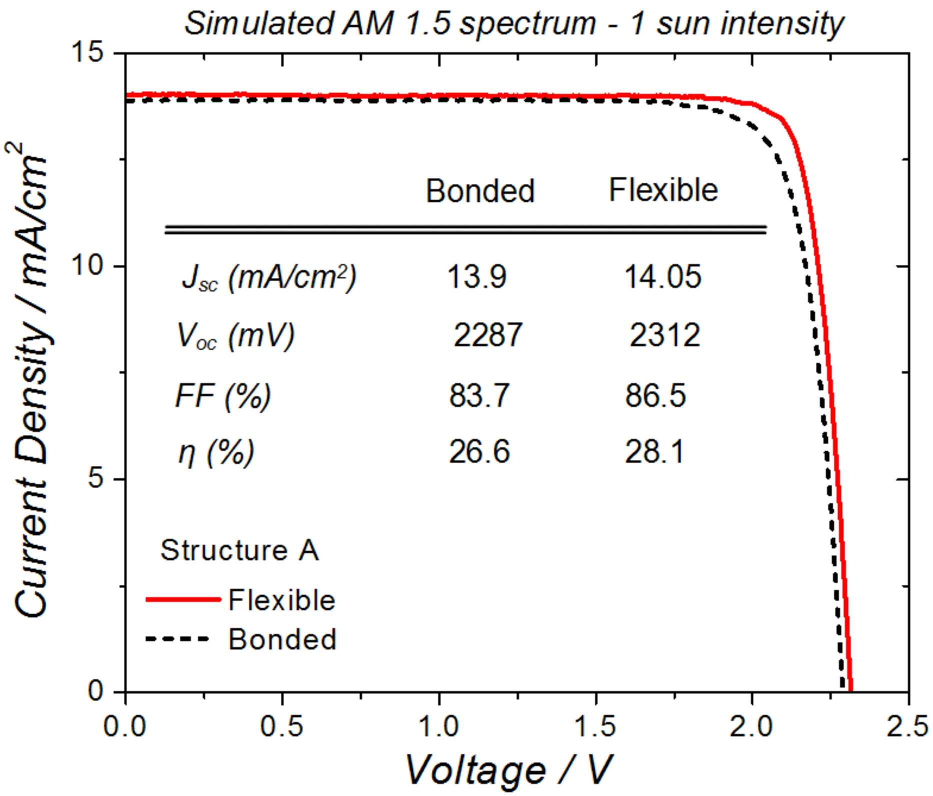
Demonstration of extremely high W/kg solar cells

Flexible inverted dual-junction III-V solar cells



Shahrjerdi et al., *Adv. Energy Mat.*, (2012)



Simulated AM 1.5 spectrum - 1 sun intensity

	Bonded	Flexible
J_{sc} (mA/cm^2)	13.9	14.05
V_{oc} (mV)	2287	2312
FF (%)	83.7	86.5
η (%)	26.6	28.1

~ 2000 W/kg specific power

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Conclusions

- High performance SSL will rely on continual improvements in many areas including thermal management, and process cost-reduction.

- Controlled spalling permits room-temperature layer removal by using intrinsically stressed surface layers to induce lateral fracture in a substrate and mechanically controlling the crack initiation and propagation.

- CST offers not only an extremely cost-effective means for GaN layer transfer, but much greater process integration flexibility as well.

- CST has been applied successfully to most major semiconductor crystals, wafers, ingots and even completed devices.

    - *The technique is general and can be applied to any brittle substrate.*

- Generalized, rigorous physical models have been developed to predict the spalling behavior of any brittle substrate / stressor combination.

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